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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

ASUS COMPUTER INTERNATIONAL,

Plaintiff,

v.

ROUND ROCK RESEARCH, LLC,

Defendant.

ROUND ROCK RESEARCH, LLC,

Counterclaim Plaintiff,

v.

ASUSTEK COMPUTER INC. and ASUS COMPUTER INTERNATIONAL

Counterclaim Defendants.

Case No. 3:12-cv-02099-JST

PLAINTIFF'S AND COUNTERCLAIM DEFENDANTS' RESPONSIVE CLAIM CONSTRUCTION BRIEF

Judge: Hon. Jon S. Tigar

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ASUSTeK Computer Inc. and ASUS Computer International (collectively "ASUS") submit this brief to address the construction of certain disputed terms in U.S. Patent Nos. 6,570,791 ("'791 patent"), 6,765,276 ("'276 patent"), 6,845,053 ("'053 patent"), 6,930,949 ("'949 patent"), 7,021,520 ("'520 patent"), and 7,279,353 ("'353 patent") (collectively "patents-in-suit").[1]

I. SUMMARY OF ARGUMENT

The parties dispute the meaning of the following terms: "bottom anti-reflection coating" in the '276 patent, "planarizing" and "over" in the '353 patent, "active standby mode" in the '949 patent, "differential voltage from the array of non-volatile memory cells" in the '791 patent, and "adjustable current consumption being set to the low power mode in response to a state of the mode control bit" in the '053 patent.[2]

ASUS's proposed constructions strictly and carefully adhere to the disclosure of the patents-in-suit and their prosecution histories. In contrast, plaintiff Round Rock Research, LLC ("Round Rock") endeavors to construe these terms in a manner that would improperly expand the claim scope – either by seeking to recapture subject matter that was disclaimed or by advancing constructions that are far beyond any supported meaning.

II. INTRODUCTION

ASUS is a worldwide leader in the field of computer systems. Round Rock, a non-practicing entity, filed a first suit against ASUS in the District of Delaware on October 14, 2011. As part of its licensing campaign, Round Rock threatened ASUS with additional patents in its portfolio. ASUS filed this declaratory judgment action against Round Rock on April 26, 2012, seeking declarations that the patents-in-suit were invalid, unenforceable, and not infringed by ASUS. Round Rock subsequently counterclaimed for infringement of these patents.

[1] The '791, '276, '053, '949, and '353 patents have been previously furnished to the court in Exhibits 1-5 of the Chang declaration.

[2] Pursuant to the Case Management Order issued by Judge Alsup on September 6, 2012 (D.I. 34), the parties were limited to proposing no more than six phrases for the first claim construction hearing. ASUS believes that there are additional terms that should be construed. With the assignment of this case to Judge Tigar, some indication of how the Court intends to address this issue would assist the parties.

III. LEGAL STANDARDS OF CLAIM CONSTRUCTION

The following discussion highlights principles of claim construction that are of particular relevance to the terms at issue.

A. The Claim Language Defines The Scope of The Invention

The scope of a patented invention is defined by the claim language.[3] As a result, it is up to the patentee to choose the words that will "particularly point out and distinctly claim the subject matter which the patentee regards as his invention."[4] The words chosen must result in a claim that is sufficiently definite, *i.e.*, such that one skilled in the art would understand the scope of the claim – as opposed to possible meanings of individual words or phrases of the claim taken in the abstract – when the claim is read in light of the rest of the specification.[5]

Accordingly, the claims "must be read in view of the specification, of which they are a part."[6] In fact, the Federal Circuit has reiterated that the specification "is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term."[7] "Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction."[8] This led the Federal Circuit to conclude that "it is therefore entirely appropriate for a court, when conducting claim construction, to rely heavily on the written description for guidance as to the meaning of claims."[9]

B. The Prosecution History Can Limit Claim Scope

The prosecution history, which contains the Applicants' statements to the Patent Office, is part of the intrinsic record and is relevant to determining "whether the inventor limited the

[3] *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 373 (1996).
[4] *Brookhill-Wilk 1, LLC. v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1298 (Fed. Cir. 2003) (citations omitted); *Helmsderfer v. Bobrick Washroom Equipment, Inc.*, 527 F.3d 1379, 1383 (Fed. Cir. 2008) ("The patentee chooses the language and accordingly the scope of his claims.").
[5] *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576 (Fed. Cir. 1986).
[6] *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005).
[7] *Id.*
[8] *Id.* at 1316.
[9] *Id.* at 1317.

invention in the course of prosecution, making the claim narrower than it would otherwise be."[10] Any scope that the applicants disclaimed in order to obtain a patent must be excluded.[11] Moreover, courts should not "construe the claims to cover subject matter broader than that which the patentee itself regarded as comprising its inventions and represented to the [Patent Office]."[12]

"[W]here the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender."[13] It is well established that "prosecution disclaimer promotes the public notice function of the intrinsic evidence and protects the public's reliance on definitive statements made during prosecution."[14] In order to limit the meaning of a claim term, a patentee's statements during prosecution need only constitute "a clear and unmistakable disavowal" of claim scope.[15] Once disclaimer is made during prosecution, it applies regardless of whether the Patent Office relied on it.[16]

C. Claim Scope Cannot Exceed The Written Description

The claims must be adequately supported by the patent's written description. If a claim does not find adequate support in the written description, it is invalid under 35 U.S.C. § 112(1). "The purpose of this provision [§ 112(1)] is to ensure that the scope of the right to exclude, as set forth in the claims, does not overreach the scope of the inventor's contribution to the field of art as described in the patent specification."[17] As a result, the scope of a properly construed claim should not exceed that of the disclosure. "Although the specification need not present every embodiment or permutation of the invention and the claims are not limited to the preferred embodiment of the invention, neither do the claims enlarge what is patented beyond what the inventor has described as the invention."[18] Thus, "in the absence of something in the written

[10] *Id.*
[11] *Id.*
[12] *Microsoft Corp. v. Multi-Tech Sys.*, 357 F.3d 1340, 1349 (Fed. Cir. 2004).
[13] *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003).
[14] *Id.*
[15] *Purdue Pharma L.P. v. Endo Pharms., Inc.*, 438 F.3d 1123, 1136 (Fed. Cir. 2006).
[16] *Microsoft*, 357 F.3d at 1350.
[17] *Reiffin v. Microsoft Corp.*, 214 F.3d 1342, 1345 (Fed. Cir. 2000).
[18] *Network, LLC v. Centraal Corp.*, 242 F.3d 1347, 1352 (Fed. Cir. 2001) (citation omitted).

description and/or prosecution history to provide explicit or implicit notice to the public—i.e., those of ordinary skill in the art—that the inventor intended a disputed term to cover more than the ordinary and customary meaning revealed by the context of the intrinsic record, it is improper to read the term to encompass a broader definition simply because it may be found in a dictionary, treatise, or other extrinsic source."[19]

IV. U.S. PATENT NO. 6,570,791 ("'791 PATENT")

A. Overview of the '791 Patent

The '791 patent relates to flash memory, a type of electronic non-volatile computer storage device that can be electrically erased and reprogrammed. Because it is non-volatile, flash memory retains stored data even after the computer is turned off. SDRAM, or synchronous dynamic random access memory, is a type of volatile memory, which means that it loses its data quickly when power is removed. SDRAM is referred to as synchronous because the memory is aligned with the computer's internal clock and transfers data in accordance with the clock signal. A particular type of SDRAM, called double data rate (DDR) DRAM, provides for faster data communications because it transfers data on both the rising *and* falling edge of a clock signal, making it essentially twice as fast as traditional SDRAM.

The '791 patent claims to provide a "flash memory [that] has an interface corresponding to a DDR DRAM," thus providing "a non-volatile memory that can communicate at DRAM speeds."[20] In particular, the '791 patent describes a new method for reading non-volatile memory cells.[21] As described in the specification of the '791 patent, in traditional flash memory cells the cells are read using a current-sensing scheme, which compares a current conducted by a memory cell to a reference current.[22] This method is described as being slower than the "differential voltage sensing scheme" used to read the DRAM memory cells[23] One aspect of the'791 patent invention is to read non-volatile memory cells using the voltage sensing technique traditionally

[19] *Nystrom v. TREX Co.*, 424 F.3d 1136, 1145 (Fed. Cir. 2005).
[20] '791 patent, Abstract, 1:34-38.
[21] *Id*., 2:44-47.
[22] *Id*., 5:10-12.
[23] *Id*., 5:7-13.

used by DRAM.[24]

B. Construction of Disputed Term(s)--Differential Voltage from the Array of Non-Volatile Memory Cells (Asserted Claims 1, 3, and 4)

ASUS's Proposed Construction	Round Rock's Proposed Construction
difference in voltage between two bit lines from the array of non-volatile memory cells	determines the difference between the voltage in the array of nonvolatile memory cells and a reference voltage

The parties' basic dispute is whether the difference in voltage referred to in the disputed claim term refers to a difference in voltage between bit lines from the array of non-volatile memory cells, or to voltage difference between a voltage in the array of non-volatile memory cells and a reference voltage. Round Rock's unidentified reference voltage apparently need not come from the array and is unsupported by the patent. The court should adopt ASUS's construction and interpret "differential voltage from the array of non-volatile memory cells" to mean "difference in voltage between two bit lines from the array of non-volatile memory cells." This construction is consistent with the claim language, the specification, and the prosecution history.

1. Claim Language Supports ASUS's Construction

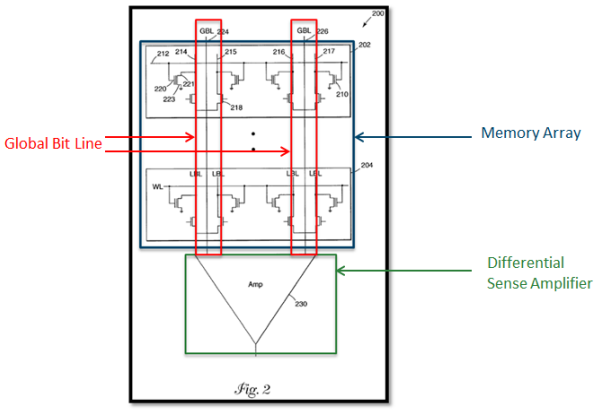
ASUS's construction is consistent with the language of the claims. For example, Claim 1 recites: "A flash memory comprising an array of non-volatile memory cells; sense amplifier circuitry ***coupled to*** the array, wherein the sense amplifier detects a differential voltage ***from the array*** of non-volatile memory cells; data connections; and output circuitry to provide output data on the data connections on rising and falling edges of a clock signal" (emphasis added). The plain reading of the claim language is that the differential voltage is detected ***from the array itself***, which in turn means that the source of the two voltages to be compared are both within the array. The fact that the sense amplifier circuitry is specified to be coupled to the array of memory cells further supports the understanding that the differential voltage is detected from the array and that the source of the two voltages to be compared are both within the array.

[24] *Id.*, 5:7-18.

2. The Specification Supports ASUS's Construction

The specification of the '791 patent further supports ASUS's construction. The embodiments described in the specification for using a voltage sensing technique to read the non-volatile memory cells all recite comparing voltages between two ***digit lines*** from within the memory array rather than between the memory array and a reference.[25] The '791 patent's use of "digit lines," as opposed to "ground" or other typical words used in the art to describe a reference voltage, highlights that for purposes of the '791 patent claims "differential voltage" are to be determined by comparison of two voltages from the memory array. This reading is further buttressed by the '791 patent's discussion of embodiments in which one of the voltage source is "pre-charged"; since such embodiments would require a voltage source that *can* be pre-charged -- such as digit lines or bit lines in a memory array -- rather than any reference voltage, such as a ground or a voltage source provided by an external power supply-- that cannot be pre-charged by the memory device.[26]

Finally, the specification supports ASUS's construction because all of the figures in the patents incorporated by reference in the '791 specification to illustrate a "voltage-sensing scheme" depict a sense amplifier that senses a differential voltage between two "global bit lines" (which are from the memory array) rather than between the array and a reference voltage as argued by Round Rock.[27] An



[25] *Id.*, 5:17-20 (describing "[a]n embodiment of the present invention [that] uses a voltage sensing technique to read the non-volatile memory cells. . . [where] differential ***digit lines*** are precharged to differential voltage levels prior to accessing a memory cell") (emphasis added); 5:19-23 (describing how an "active ***digit line*** that is coupled to a read memory cell can be pre-charged to a voltage that is greater than a complementary ***digit line***") (emphasis added); 5:28-20 (stating that the "differential voltage sensing circuit can be used to detect and amplify the ***digit line*** voltages") (emphasis added). Digit lines are synonymous with bit lines.

[26] A person having ordinary skill in the art would understand that, for a digit line to be "precharged," it must be associated with a capacitive element or a memory cell.

[27] *Id.*, 2:47-55. *See also* Exs. A-D (U.S. Patent No. 6,496,434 ("the '434 patent"), U.S. Patent No. 6,327,202 ("the '202 patent"), U.S. Patent No. 6,3010,809 ("the '809 patent"), and U.S. Patent No. 6,507,525 ("the '525 patent"), each having substantially similar figures. Except where

exemplary figure from these incorporated patents (FIG. 2 of U.S. Patent No. 6,327,202) is show to the right.

3. Round Rock's Proposed Construction Comparing a Voltage From The Memory Array with a Reference Voltage is Inconsistent with Intrinsic Evidence

As discussed above, asserted claims 1, 3, and 4 distinctly recite a differential voltage ***from the array of non-volatile memory cells***. Round Rock's construction impermissibly seeks to read out "from the array of non-volatile memory cells" from the claims. Neither can Round Rock point to anything in the specification that supports their construction. For example, Round Rock cites to the portion of the specification that describes conventional flash memories as reading memory cells by using a current sensing technique that senses a reference current. (Round Rock Claim Construction Br., at 13). This portion of the specification, however, describes ***prior art***, not the invention. Indeed, this section of the specification supports ASUS's construction of the disputed phrase, as it contrasts the "differential-voltage sensing scheme" at issue in the disputed claim term with the slower "current sensing technique." *Id.*, 5:7-13.

4. Constructions as They Relate to Summary Judgment[28]

Round Rock has not shown that the accused products, including eMMC NAND Flash, detect differential voltages from the memory array. Thus, to the extent ASUS's construction is adopted, summary judgment would be proper at least as to those claim terms of the '791 patent containing the limitation of "differential voltage from the array of non-volatile memory cells."

V. U.S. PATENT NO. 6,765,276

A. Overview of the '276 Patent

The '276 patent relates to image sensors for use in digital imaging systems. The image sensors are used to capture images, and they typically include an array of pixels, each of which contains a light-sensing element. In color applications, the pixel sensor elements typically

otherwise noted, all exhibits are attached to the Declaration of Tawen Chang in Support of ASUS's Responsive Claim Construction Brief.

[28] ASUS provides this precis of the eventual summary-judgment issues and how claim construction differences may affect summary judgment pursuant to Judge Alsup's September 6, 2012 Case Management Order. (D.I. 34.)

receives light through a color filter, which only allows radiation of certain wavelengths to pass through. This allows the image sensors to capture color information, since different wavelengths corresponds to different colors.

In particular, the '276 patent describes a bottom anti-reflection coating ("BARC") layer that protects areas of the active image sensing device structure during formation of the color filter array on top of the active image sensing device. '276 patent, Abstract. This preserves the intrinsic transmission characteristics of the active image sensing device structure. *Id*. The '276 patent also describes the BARC as performing additional functions. For instance, in some embodiments BARC improves the optical transmission characteristics of one or more colors of the color filter array.[29]

B. Bottom Anti-Reflection Coating (Asserted Claims 1, 3, 5, 8, 9 and 11)

ASUS's Proposed Construction	Round Rock's Proposed Construction
a coating that is disposed between a patterning resist layer and underlying reflective structures to enhance control of critical dimensions in the patterning resist layer by suppressing reflective notching, standing wave effects, and the swing ratio caused by thin film interference	a coating that has an index of refraction, an extinction coefficient, and a thickness

The court should adopt ASUS's construction of "bottom anti-reflection coating" ("BARC"): "a coating that is disposed between a patterning resist layer and underlying reflective structures to enhance control of critical dimensions in the patterning resist layer by suppressing reflective notching, standing wave effects, and the swing ratio caused by thin film interference." ASUS's construction is supported by the specification and patentee defined BARC in this manner during prosecution of the '276 patent in order to distinguish prior art.

1. ASUS's Construction of BARC Is Identical to the Definition Patentee Used to Overcome Prior Art During Prosecution

During prosecution of the '276 patent, the Examiner rejected the then-pending claims as either anticipated by or rendered obvious by 6,184,055 ("Yang") and U.S. Patent Nos. 5,654,202

[29] *See, e.g, id*., 4:45-51 ("[T]he BARC layer thickness may be selected so that the peak transmission at one or more target wavelengths is increased relative to device structures that do not include BARC layer….").

("Daly"). In attempting to overcome the rejection, the applicant argued that these prior art references did not teach a BARC. Specifically, the applicant argued that BARC is a "well-known" term of art with a commonly understood meaning:

> A bottom antireflection coating is a well-known term of art that refers to ***a coating that is disposed between a patterning resist layer and underlying reflective structures to enhance control of critical dimensions in the patterning resist layer by suppressing reflective notching, standing wave effects, and the swing ratio caused by thin film interference***. A bottom antireflection coating may suppress unwanted resist-activating radiation by absorption or wave cancellation, or both."[30]

The applicants then tried to use this definition to distinguish Daly, stating:

> There is no hint in Daly that planarization layer 18 operates as a bottom antireflection coating that ***enhances control of critical dimensions in an overlying patterning resist layer by suppressing reflective notching, standing wave effects, and the swing ratio caused by thin film interference***. …. Daly does not teach or suggest anything about bottom antireflection coatings, much less that planarization layer 18 could be a bottom antireflection coating. *Id.*, 3 (emphasis added).

On December 4, 2002, the Examiner again rejected the pending claims over Daly and Yang. The Examiner recognized that the applicant had defined BARC as "a layer that may suppress unwanted resist-activating radiation by absorption or wave cancellation or both," but nevertheless believed that Daly and Yang taught the use of a BARC.[31]

In response, the applicant reemphasized that in order for a layer to operate as a BARC, it is not sufficient simply for the layer to be "transparent to light within an operating wavelength range," as was the passivation layer disclosed in Yang. Rather, the applicant stated that while the specification does teach a preferred BARC layer that is "substantially absorptive of radiation in the wavelength range used to pattern color filter array … and is substantially transmissive of radiation in the wavelength range to be imaged by image sensor …," to be a BARC layer requires more:

> Applicant's specification teaches that, in some embodiments, 'BARC layer 16 preferably is substantially absorptive of radiation in the wavelength range used to pattern color filter array 14 and is substantially transmissive of radiation in the wavelength range to be imaged by image sensor 10' (page 6, lines 14-17) Such a BARC layer is perfectly consistent with the description of ***a bottom antireflection coating as a coating that is disposed between a patterning resist layer and underlying***

[30] Ex. E, Sep. 11, 2002 Amendment, at 2 (emphasis added).
[31] Ex. F, Dec. 4, 2012 Final Rejection, at 2-3.

> ***reflective structures to enhance control of critical dimensions in the patterning resist layer by suppressing reflective notching, standing wave effects, and the swing ratio caused by thin film interference.*** The mere fact that Yang's passivation layer is transparent to light within an operating wavelength range does not suggest that the passivation layer operates as a bottom antireflection coating."Ex. G, February 10, 2003 Amendment, at 4-5 (emphasis added).

Ultimately, the Examiner withdrew the anticipatory rejections of the application based on Yang and Daly.[32] A notice of allowance was issued subsequently on March 12, 2004.

As shown above, the patentee distinguished Yang and Daly by using a particular definition of BARC, which it argued to be ordinary meaning. Accordingly, ASUS's construction of BARC, which is identifcal to the definition the patentee provided during prosecution, should be adopted.

2. Round Rock's Construction Is Impermissibly Broad

Round Rock's construction of BARC is "a coating that has an index of refraction, an extinction coefficient, and a thickness." Because ***all*** materials have an index of refraction, an extinction coefficient,m and a thickness, Round Rock's construction in effect recites "a coating."

Indeed, Round Rock ***admits*** as much in its briefing. For example, Round Rock explains in its opening brief that "any substance would be assigned an index of refraction." (Round Rock Opening Claim Construction Br., at 9). In describing the "extinction coefficient," Round Rock states that "one of skill in the art would understand this to be another measureable optical property relating to light absorption and the index of refraction." *Id.* Similarly, it is self-evident that any coating would have a thickness.

Round Rock's construction is impermissibly broad. It reads out "bottom" and "anti-reflective" from the claim term "bottom anti-reflective coating" and strips the term of all meaning. Such a construction is particularly unacceptable because of the clear definition of BARC used in prosecution to distinguish the prior art -- a definition the patentee itself acknowledged to be the ordinary meaning.

3. Constructions as They Relate to Summary Judgment

Round Rock asserts that the OmniVision sensor in the ASUS Eee Slate EP121 infringes

[32] Ex. H, '276 Prosecution, June 19, 2003 Non-Final Rejection at 2.

its patent. Without any analysis, Round Rock states that a layer of the OV273AB sensor is a BARC. Round Rock has shown no evidence that the layer it accuses meets the definition of BARC as properly construed by ASUS. Thus, to the extent ASUS's construction is adopted, summary judgment of non-infringement would be appropriate for all asserted claims. In addition, Round Rock's construction is so broad that, to the extent it is adopted by the Court, summary judgment of invalidity would likely be appropriate for one or more asserted claims.

VI. UNITED STATES PATENT NO. 7,279,353 ("'353 PATENT")

A. Overview of the '353 Patent

The '353 patent relates to an method for forming a pixel cell. Typical prior art devices, as described by the patent, had non-uniform passivation layers (i.e., protective layers) formed over final metallization layers and this non-uniformity resulted in contaminants leaking into the final metallization layer. To remedy this problem, the '353 patent describes an imaging element where "[a] pixel cell is formed by locating a first passivation layer over the final layer of metal lines. Subsequently, the uneven, non-uniform passivation layer is subjected to a planarization process such as chemical mechanical polishing, mechanical abrasion, or etching. . . Once a uniform, flat first passivation layer is achieved over the final metal, a second passivation layer, a color filter array, or a lens forming layer with uniform thickness is formed over the first passivation layer." '353 patent, Abstract. The color filter layer array also undergoes a "planarization process prior to formation of the lens forming layer." *Id.; see also* Independent Claims 1, 13, and 20.

B. "Planarizing" (Asserted Claims 1, 3, 5, 13-17, and 20)

ASUS's Proposed Construction	Round Rock's Proposed Construction
"uniformly flattening"	Plain meaning, or, in the alternative: "processing or preparing by eliminating convex and/or concave regions"

The court should construe "planarizing" to mean "uniformly flattening." This construction is consistent with the claims, the specification, and the prosecution history.

1. The Specification Describes Planarizing as "Uniformly Flattening"

ASUS's construction is supported by the specification, which consistently recites the

planarizing step as uniformly flattening. For example, the Abstract describes the formation of a first passivation layer over a final metallization layer as follows: "Subsequently, the uneven, non-uniform passivation layer is subject to a planarization process. . . Once a ***uniform, flat*** first passivation layer is achieved" another layer with "uniform thickness is formed over the passivation layer."[33]

The specification further supports ASUS's construction because it describes a non-uniform, "bread-loaf[ed]" passivation layer as the problem in the prior art that the '353 patent is trying to solve, and emphasizes uniform flattening of the passivation layer as the solution. For instance, the background section of the '353 patent states that, in the prior art:

> A passivation layer is also typically deposited over the final metallization layer … This deposition may cause a ***"bread-loafing effect"*** above the metal lines … Accordingly, a ***non-uniform passivation layer is produced***, which may cause a non-uniform floor for a subsequent filter array coating, which may in turn lead to stress-induced striations, poor color performance and low predictability of the overall image captured by the pixel cell array.[34]

It then states that "***a more uniform, flat*** oxide passivation layer over the final layer of metal lines will allow for a much thinner nitride passivation deposition, reducing stress in the structure of the passivation layer of the pixel cell."[35] Finally, it goes on to describe the invention of the '353 patent as follows:

> The present invention provides a more ***uniform*** upper surface for the passivation layer deposited over the final layer of metal lines by post-deposition surface treating, e.g., by chemical mechanical polishing the passivation layer. As a result, subsequent layers deposited over the passivation layer, such as other passivation layers or a color filter array, can be formed with a ***more uniform thickness***, decreasing the possibility of stress-induced defects and ion contamination.[36]

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[33] *See* '353 Patent, Abstract.

[34] *Id*., 1:30-40 (emphasis added); *see also id*. at 3:59-61 ("The oxide passivation layer surface … may have an uneven surface because of the presence of the metal lines in the upper metallization layer."); 4:7-12 ("The non-uniform thickness of nitride passivation layer 21 can lead to the formation of keyholes 26 between the metal lines where … deteriorating elements can penetrate the nitride passivation layer 21. The non-uniform thickness of nitride passivation layer 21 can also create stress within the layer itself, … , making it prone to cracking.").

[35] *Id*., 1:54-58 (emphasis added).

[36] *Id*., 1:63-2:2 (emphasis added). *See also id*. at 4:65-67 ("To avoid the formation of keyholes 26 and to achieve a ***more uniform*** nitride passivation layer, it would be desirable to treat the upper surface 15 of oxide passivation layer 11 to produce a ***flat*** surface on which to subsequently deposit a nitride passivation layer. ***The desired flat upper surface 10 can be achieved by a planarization process***.") (emphasis added); 5:19-22 ("Because the oxide passivation layer surface 10 is ***flat***, the nitride passivation layer 21 likewise has a ***flat*** upper surface 20, thereby eliminating the formation of keyholes 26….") (emphasis added); 5:23-

Indeed, all embodiments of the '353 patent invention disclosed in the specification describe creating a surface that is uniformly flattened through planarization.[37]

2. Round Rock's Construction is Inconsistent with the Intrinsic Evidence

Round Rock's construction of "planarizing" as "processing or preparing by eliminating convex and/or concave regions" is inconsistent with intrinsic evidence. For example, the construction makes no distinction between elimination of convex and/or concave regions through filling the concave regions as opposed to the flattening of the regions. However, claims 1 and 14 recite in part "forming a passivation layer over a final metallization layer," "planarizing a surface of said passivation layer," and "stopping said planarizing before reaching said final metallization layer." That the claim requires the planarization of the passivation layer to be stopped before reaching the final metallization layer below the passivation layer shows that planarizing is a flattening process in which material is removed (e.g., via chemical mechanical polishing), not a process of filling out the concave regions.[38]

In fact, although the '353 patent does discuss "spin-on-glass," which is a process that "fills in" concave regions, in the context of creating different layers during the manufacture of an imaging element, the patent does not describe such a process as "planarizing." Instead, the '353 patent describes the "spin-on glass layer" created through such a process as part of a layer that can later be planarized:

> In another embodiment of the invention shown in FIG. 7, a flowable material such as a spin-on-glass material may be applied to the oxide passivation layer 11, then heated to form a spin-on glass layer 12 over the oxide passivation layer 11 such that the spin-on-glass material fills the "valley" regions 17 and covers the "bread-loaf" regions 16. ***The spin-on-glass layer 12 and the "bread-loaf" regions 16 may be planarized*** together by CMP or dry etchback according to known techniques.[39]

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25 ("Furthermore, the nitride passivation layer 21 has ***uniform*** thickness and may be thinner than would be required if it had a non-uniform surface 25.") (emphasis added); 5:53-54 ("Because the resulting surface 13 is ***flat***, the nitride passivation layer 21 likewise has a ***flat*** upper surface.") (emphasis added); 6:2-28 ("Nitride passivation layer 21 is then ***planarized to produce a flat upper surface***.") (emphasis added).

[37] *Id*.

[38] *See, e.g., id*, Fig. 3 and 4; *see also id.* at 5:7-8 ("In a preferred embodiment, CMP [chemical mechanical polishing] is performed after deposition of the oxide passivation material.")

[39] *See id*. at 5:36-46 (emphasis added); *see also id*., claim 12.

3. Constructions as They Relate to Summary Judgment

Round Rock is asserting that CMOS sensors used in ASUS's products infringe. More particularly, Round Rock alleges that elements of the CMOS sensors are planarized. The accused elements of the CMOS sensors are not uniformly flattened. Thus, to the extent that the Court adopts ASUS's proper construction of "planarizing," summary judgment of non-infringement would be appropriate with respect to the asserted claims of the '353 patent.

C. "Over" (Asserted Claims 1, 13, 20-21)

ASUS's Proposed Construction	Round Rock's Proposed Construction
on top of and without intervening structures	Plain meaning, or, in the alternative, "above"

The court should construe "over" to mean "on top of and without intervening structures." This construction is consistent with the claims, the specification, and the prosecution history.

1. ASUS's Construction Is Consistent With Ordinary Meaning in Light of the Specification

As an initial matter, "over" is a term with multiple ordinary meanings depending on the context of its use. Thus, in construing the term it is particularly important to interpret "over" in the context of the specification. In this case, the claim language requires a method of forming a semiconductor device that "provide a passivation layer located ***over*** a final metallization layer."[40] As discussed further below, the specification makes clear that the passivation layer serves a protective function with respect to the metallization layer, which in turn requires the passivation layer to be directly on top of the final metallization layer. Thus, ordinary meaning of the term "over" in the context of the '353 patent specification supports ASUS's construction.

The passivation layer, as known in the art, is provided to protect the metallization layer from contaminants.[41] The '353 patent specification also makes clear the protective function of the passivation layer. As discussed in the background of the '353 patent, the problem that the '353 patent was trying to solve involved weak passivation layers, such as "bread-loafed" passivation layers, that allows contaminants to penetrate into the silicone region of the imaging

[40] *See id*., claim 1.
[41] *See, e.g., id.*, at 1:46-49 ("Where nitride coverage is thin, or weak, mobile contaminants … can penetrate into the silicon device region and cause loss of pixel functionality.")

device.[42] The invention purported to provide a more robust passivation layer that provides greater protection for the layer of metal lines beneath it.[43]

To serve its protective function, the passivation layer must be ***directly over*** the final metallization layer.[44] For example, the specification states that "[t]he present invention provides a more uniform upper surface for the passivation layer deposited ***over*** the final layer of metal lines . . . ***decreasing the possibility of stress-induced defects and ion contamination***." *See* '353 patent, 1:62-2:2. This is further consistent with all the embodiments in the '353 patent. For example, all figures illustrating a passivation layer over the metallization layer show a passivation layer that is directly on top of the metallization layer without intervening structures.[45] In short, the passivation layer is disposed above the final metallization layer to protect it; accordingly, it is essential that it be "on top of [the metallization layer] … without intervening structures" consistent with ASUS's construction of the term "over."

2. Round Rock's Construction is Not Supported by The Specification

Round Rock argues that "over" should be construed to mean "above." Round Rock's construction ignores the context of how the term is used in the claims and the specification. As previously stated, the specification provides the passivation layer over the final metallization layer for protection. The specification does not describe the passivation layer as "above" the final metallization layer allowing for intervening structures. This would leave the final metallization layer unprotected and open to contaminants. Round Rock's construction is a departure from common practice in the art and a departure from the purpose and disclosure of the specification.

Accordingly, ASUS's construction of "over" to be "on top of and without intervening structures" is correct and should be adopted.

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[42] *See id.*, 1:30-33 (describing the problem of bread-loafed passivation layers); 1:43-46.
[43] *See id.*, 1:54-58 (describing "a more uniform, flat oxide passivation layer over the final layer of metal lines [that] will allow for a much thinner nitride passivation deposition, reducing stress in the structure of the passivation layer of the pixel cell.").
[44] Passivation layers are well known and used in the art to protect substances from contaminants. See, e.g., Ex. I, McGraw Hill Dictionary of Scientific and Technical Terms (5th ed. 1994) at 1455 ("passivation … Growth of an oxide layer on the surface of a semiconductor to provide electrical stability by isolating the transistor surface from electrical and chemical conditions in the environment; this reduces reverse-current leakage, increases breakdown voltage, and raises power dissipation rating….").
[45] *See, e.g., id.*, '353 patent, Figs. 2-10 (Oxide Passivation Layer 11).

3. Constructions as they relate to summary judgment

Round Rock proposed the term "over" for construction at the hearing. ASUS is still investigating its defenses and the proper construction of this term may impact these defenses. It is notable, moreover, that Round Rock is currently alleging infringement inconsistently across two patents (e.g., accusing a polymer of being part of the color filter array in one instance and as part of the BARC in another.) A proper construction of "over" may require Round Rock to provide a more definite infringement contention.

VII. UNITED STATES PATENT NO. 6,930,949 ("'949 PATENT")

A. Overview of the '949 Patent

Typical memories utilize one or more delay compensation circuits. '949 patent at 1:14-20. The delay compensation circuits are used to compensate for clock signal variations. *Id.*, 1:43-40. However, "[r]unning of the delay compensation circuit during active power-down mode is a principal reason for [] additional power consumption." *Id.*, 3:45-47. One possible solution is to suspend the delay compensation circuit during power down. *Id.*, 3:58-67. However, the then JEDEC standards were incompatible with this solution. *Id.*, 4:5-6. To solve this problem, the '949 patent provides an "apparatus . . . for reducing the power consumed by a memory device [by] selectively activat[ing] a power saving mode in which operation of a delay compensation circuit may be suspended during an active power down mode of operation." *Id.*, Abstract.

B. "Active Standby Mode" (Asserted Claims 5-7, 20)

ASUS's Proposed Construction	Round Rock's Proposed Construction
"mode where a delay compensation circuit is suspended in active power down mode"	"the mode when CKE is high and there is at least one row active in any memory bank."

The court should construe "active standby mode" to mean "mode where a delay compensation circuit is suspended in active power down mode." This construction is consistent with the specification, file history, and claims.

1. ASUS's Construction is Supported by The Specification

The purpose of the '949 patent invention is to decrease power consumption by reducing

current usage in active-power down mode. This is accomplished by suspending the delay compensation circuit during active-power down mode. The Abstract of the invention describes "a memory device selectively activat[ing] a power saving mode in which operation of a delay compensation circuit may be suspended during an active power down mode of operation." *Id.*, Abstract. This is consistent with the title: "power savings in active standby mode."[46]

The specification describes two different types of power-down mode that have different associated current consumptions. "Precharge power-down" "occurs when all banks are idle" when "CKE is registered LOW." *Id.*, 3:28-32. "During a precharge power-down, a typical 4 bank memory device requires approximately 3-5 mA of current." *Id.*, 3:39-42. "Active power-down" "occurs when there is a row active in any memory bank" when "CKE is registered LOW." *Id.*, 3:27-33. Active power-down "typically [draws] 20mA." *Id.*, 3:44.

The invention is applicable to types of random access memories "that utilize one or more delay compensation circuits such as, for example, one or more delay locked loops (DLLs)." *Id.*, 1:19-21. The delay compensation circuit compensates for variations caused by changes in temperature, voltage, process variables, and loading conditions. *See id.*, 1:34-43. The delay compensation circuit consumes a considerable amount of power. *See id.*, 1:43-47 ("A delay compensation circuit typically includes a relatively large number of delay logic gates that toggle or transition with each transition of the external clock. Power is consumed when the gates transition.").

"Running of the delay compensation circuit during active power-down mode is a principal reason for the additional power consumption." *Id.*, 3:45-47. "One solution that has been proposed to the problem of minimizing the power consumed while a memory device is in power-down or standby mode involves freezing … the delay compensation circuit." *Id.*, 3:48-51. The

[46] *See also* '949 patent, 4:11-15 ("If it is possible in a given application or design to allow for more than one clock cycle on exit of an ***active power-down mode***, then, according to be[sic] present invention, ***power consumption may be reduced from the typical 20 mA per device to about 3 to 5 mA***.") (emphasis added). In its infringement contentions, Round Rock focuses on another mode called "precharge power-down mode." However, the precharge power-down mode is described as "requiring approximately 3-5 mA of current." *Id.*, 3:39-41. Accordingly, it is clear that the patent is directed towards power savings in active power down, not precharge power-down.

proposed solution "discusses suspending or freezing the delay elements of a DLL delay compensation circuit by operating a switch to prevent the external clock signal from reaching the DLL during a power-down mode of operation." *Id.,* 3:62-65.

"[I]n order to reactivate a suspended DLL or other clocked delay-line-based delay compensation circuit by reintroducing the clock signal prior to exiting active standby mode, more than one clock cycle is needed for reliability." *Id.*, 4:1-5. "If it is possible in a given or design to allow for more than one clock cycle on exit of an active power-down mode, then, according to be [sic] present invention, power consumption may be reduced from the typical 20 mA per device to about 3 to 5 mA." *Id.*, 4:10-15.

"In some standby modes of operation, such as in the active power-down mode, the time it takes to resynchronize or recalibrate the delay compensation circuit after a power-down is not acceptable." *Id.*, 1:53-58. "[A] complete power-down of a DLL or other delay compensation circuit during a power-down mode is impractical due to the number of cycles needed to resynchronize or recalibrate the circuit with the clock when it is restarted." *Id.*, 3:58-61. This is because this solution "unfortunately conflicts with the JEDEC standard." *Id.*, 4:5-6. Therefore, the power savings mode is "provided as an optional programmable feature… [to be] backwards compatible with the JEDEC standard." *Id.*, 4:20-22.

Thus, the invention describes a power saving mode that involves suspending the delay compensation circuit in active-power down mode to reduce the 20 mA current consumption to about 3 to 5 mA.

2. Round Rock's Construction is Unsupported by the Specification

Nowhere in the specification is there support for Round Rock's construction. For example, Round Rock cites to the following portion of the '949 patent: "As FIG. 5a shows, the DRAM will exit power-down mode in one clock cycle when CKE 512 is again high on the next CK 510 transition high thus maintaining compliance with the JEDEC standards." '949 patent at 5:14-17. However, this citation discusses the JEDEC standard as exiting a power-down mode in one clock cycle. *See, e.g.,* 4:5-11 ("This unfortunately conflicts with the JEDEC standard. In

many cases ***compliance with the JEDEC clock requirement may not be as important to designers as achieving power savings in active power-down mode***.) (emphasis added)

Indeed, Figure 5a illustrates the incorrectness of Round Rock's construction. For example, "the mode when CKE is high and there is at least one row active in any memory bank" reads on embodiments outside of and not associated with power-down mode (i.e., it reads on a mode of normal memory operation). This construction is beyond the scope of the specification.

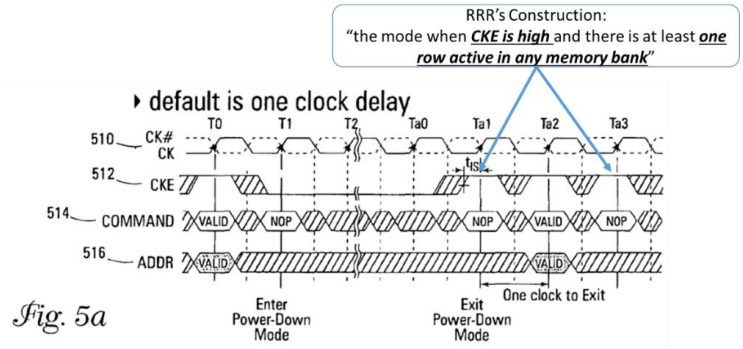


Fig. 5a

Further, Round Rock states that column 3, lines 30-34 supports its proposition that "the specification further explains that an 'active' state occurs when 'there is a row active in any memory bank' when DRAM transition into either standby or power-down mode." (Round Rock Claim Construction Br. at 13.) This passage discusses "precharge power-down" and "active power-down" where only "active power-down" is the power down mode associated with "at least one row active in any memory bank." *See Id.*, 3:30-34. Nothing in this citation supports Round Rock's construction for ***active standby mode***. Round Rock further cites to a document submitted in an information disclosure statement. (Round Rock Claim Construction Br. at 14.) The document provides an "active standby current" but does not describe the parameters for the "active standby mode." Again, nothing within this document supports the broad construction of active standby mode that Round Rock is seeking.

Finally, Round Rock's proposed construction is directly contradictory to its infringement contentions. Ex. J. Specifically, Round Rock's proposed constructions requires CKE to be high in active standby mode. However, in its infringement contentions, it points to pre-charge power down mode as meeting the active standby mode limitation. CKE is low in pre-charge power down mode, however, as shown in figure below:

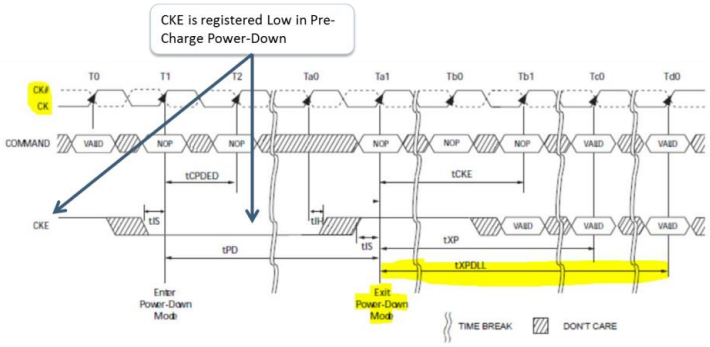


Figure 68 — Precharge Power-Down (Slow Exit Mode) Entry and Exit

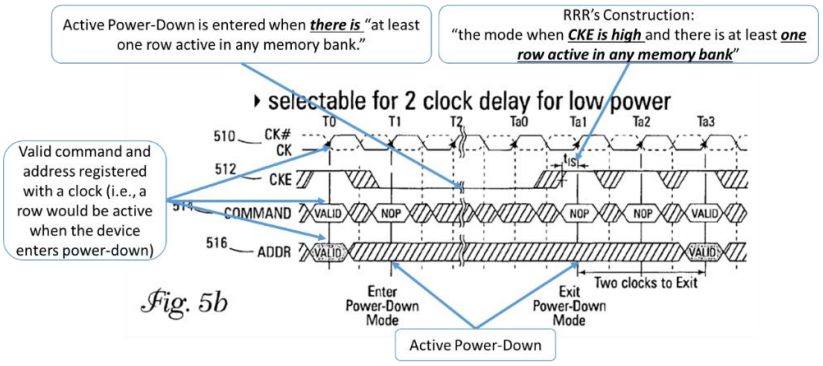
(*Id.*, Page 17) (Emphasis Round Rock's infringement contentions)

3. The "Active Standby Mode" Described in the Claims is Associated with the "Active Power-Down Mode"

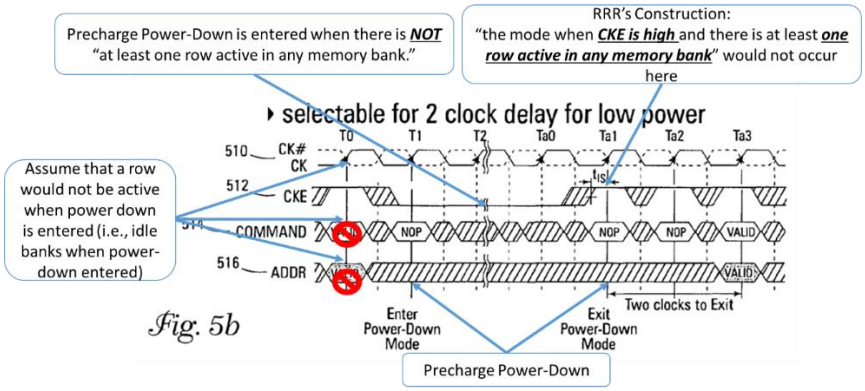
Claim 5 recites: "a mode of operation wherein a transition from an active standby mode to a normal operation mode takes place in a period of more than one clock cycle." The power savings mode of operation contemplated by the invention is where "operation of a delay compensation circuit [that] ***may be suspended during an active power down mode*** of operation." '949 patent, Abstract (emphasis added). As previously stated, the prior art described the problem: "[r]unning of the delay compensation circuit during active-power down mode is a ***principal reason*** for the additional power consumption." *Id.*, 3:45-47 (emphasis added). ASUS's construction properly considers the power savings mode disclosed: an active power down mode where the delay compensation circuit is disabled.

In fact, Round Rock's construction highlights the association of the active power-down mode with the active standby mode. For example, Round Rock's construction recognizes that the active standby mode discussed in the patent is associated with active power-down when it states that active standby mode requires that "there is at least one row active in any memory bank." As previously discussed, there are two power down modes recognized by the specification: (i) pre-charge power-down; and (ii) active power-down. *See id.*, 3:30-34. "[I]f power-down occurs when there is a row active in any memory bank, this mode is referred to as "active power-down." *See id.*, 3:32-34. Round Rock's defined version of "active standby mode" can only be associated with "active power-down mode." ASUS's construction makes this distinction more clearly and

precisely without the impermissible broadness of Round Rock's construction.[47]



Round Rock's construction further highlights the association of active power-down with the claimed active standby mode when one imagines that Fig. 5b illustrates entering power down-mode when there is not any rows active in the memory bank (i.e., precharge power-down).



4. Constructions as They Relate to Summary Judgment

In its infringement contentions, Round Rock has pointed to no mode in the accused products where a delay compensation circuit is suspended in active power down mode. Thus, if ASUS's correct construction of active standby mode is adopted, summary judgment of non-infringement would be appropriate as to all asserted claims containing the term "active standby mode."

VIII. U.S. PATENT NO. 6,845,053 ("'053 PATENT")

A. Overview of The '053 Patent

Prior art chip designers, as explained by the '053 patent, had to make restrictive choices in

[47] Round Rock states that ASUS "conflates" the two terms. *See* Round Rock Claim Construction at 14. ASUS's construction keeps the proper association between the active standby mode and active power-down mode whereas Round Rock's construction seeks to disassociate the active standby mode from any power-down mode.

their designs associated with programming speed and current consumption (i.e., the higher the programming speed the more the current consumed). *Id.*, 1:23-23. Some devices would benefit from a higher programming rate whereas others would benefit from less current consumption. *Id.*, at 1:29-32.

To prevent designers having to make the trade-offs at design time, the '353 patent provides "a [single] memory device that has a plurality of modes including a high data throughput mode and a low power mode." *Id.*, 1:40-42. "The state of the mode control bit selects one of the modes. In one embodiment, the mode control bit controls the rate at which data is programmed into the memory device's memory array, thereby controlling the power consumption." *Id.*, 1:42-48. "[T]he quantity of bits being programmed [can vary] in order to vary the current consumption of the memory device.

In a high throughput, higher power mode, the maximum quantity of bits is programmed at once. . . In the lower power, lower throughput mode, a reduced quantity of bits is programmed at once." *Id.*, 3:22-25. For example, multiple data select lines (DATASEL0-DATASEL3) which, depending on the state of a mode control bit (TP BIT 406), selects different blocks of data to be loaded onto a data driver 380. *See id.*, 4:13-19. The figure provided to the right illustrates the reduction of data throughput by selectively turning on/off data select lines (on illustrates when the DATASEL# line has activated writing to the drivers.

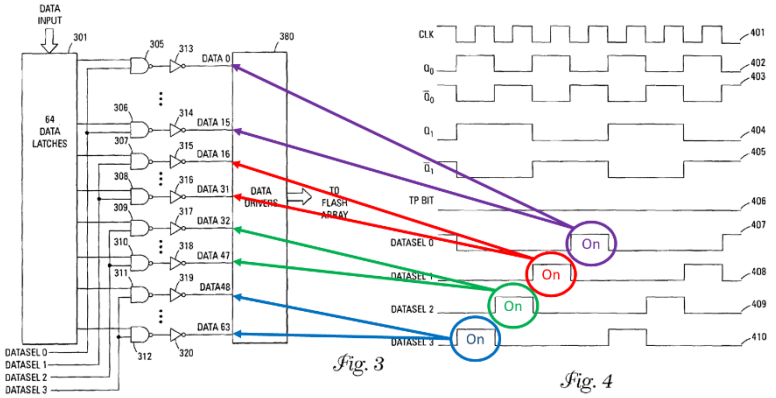


Fig. 3 *Fig. 4*

B. "adjustable current consumption being set to the low power mode in response to a state of the mode control bit" (Asserted claim 1)

ASUS's Proposed Construction	Round Rock's Proposed Construction
"the amount of current consumed being dependent on the chosen mode as determined by the state of a mode	Round Rock proposed the phrase "adjustable current consumption being set to the low power mode" for construction. They believe that the correct term for

control bit, where the mode chosen is one in which a reduced quantity of bits is programmed at once."	construction is "adjustable current consumption being set to the low power mode" and should be: Plain meaning, or, in the alternative: "setting the device to a mode for low current consumption"

The court should construe "adjustable current consumption being set to the low power mode in response to a state of the mode control bit" to mean "the amount of current consumed being dependent on the chosen mode as determined by the state of a mode control bit, where the mode chosen is one in which a reduced quantity of bits is programmed at once." This construction is consistent with the claims, the specification, and the prosecution history.

1. The specification describes a mode control bit that selects a lower data throughput

The specification supports ASUS's construction. For example, the specification describes the selection of a low power mode to achieve low current consumption (i.e., "adjustable current consumption"). *See id.,* 1:40-48 ("The embodiments of the present invention encompass a memory device that has a plurality of modes including a ***high data throughput mode and a low power mode. . . [where a] state of [a] mode control bit selects one of the modes***. In one embodiment, the mode control bit controls the rate at which data is programmed into the memory device's memory array, thereby controlling the power consumption.") (emphasis added) This allows "a memory device manufacturer with the ability to design one flash memory device that has ***a selectable low current consumption (i.e., low power) mode and a high data throughput mode***. The mode is selectable by a latch that is programmed to select one of the modes." *Id.,* 1:66-2:5 (emphasis added). All embodiments of the specification describe the low power mode as a mode that reduces the programming rate to save power (i.e., the specification always describes a high-power high data throughput mode and its converse, the low power mode). For example, the specification states:

- "…***logical 0 to instruct the memory device to enter a low power mode. A logical 1 programs the device to a high throughput mode***…" *Id.,* 3:1-4
- " ***varies the quantity of bits being programmed*** in order to vary the current consumption of the memory device. In a high throughput, higher power mode, the maximum quantity bits is programmed at once. This mode has an increased current consumption due to programming a large number of bits simultaneously. ***In the lower power, low throughput mode, a reduced***

quantity of bits is programmed at once. In this mode, the programming rate is slowed down. This reduces the current consumption of the memory device." *Id.*, 3:22-31 (emphasis added). .

- "***[I]n the low power mode, each of the data select signals is only high for one clock cycle***. During this clock cycle, the programming sequence for that data will be executed. . . In the high data throughput mode, the data select signals are always high so that all 64 data bits are written simultaneously." *Id.*, 4:48-51 (emphasis added). .
- "Other embodiments may use ***different sizes of data blocks or a different total quantity of bits*** to be programmed, depending on the application. Still other embodiments use different methods for varying the current use by the memory device. For example, setting the mode control bit to a low power mode may increase the time between programming pulses such that ***data throughput is reduced***." *Id.*, 5:3-9 (emphasis added). .
- Figure 5 describes "data throughput adjustment method… [where] [t]he mode is selected (501) based on the application for the memory device. If the device is to be used in a battery-powered device, ***low power operation would be desirable***. If the device is to be used in a line power application, ***high data throughput may be chosen*** since current consumption is not typically a concern." *Id.*, 5:21-27 (emphasis added).
- "In summary, a non-volatile memory bit is used to ***adjust the data throughput***, and therefore, the power consumption of a memory device." *Id.*, 5:42-46 (emphasis added).
- In one embodiment, the mode control bit selects a low power mode. ***This mode slows down the programming rate of the memory device***, thus reducing the current requirements." *Id.*, 5:47-50 (emphasis added).

2. The Specification does not Support Round Rock's Construction

Round Rock's citation to the specification supports ASUS's construction. For example, Round Rock states that "setting the mode control bit to a low power mode reduces the current consumption by, for example, ***reducing the memory device data programming rate***." Round Rock Claim Construction Br., at 20 (emphasis added). Round Rock's citation to the specification discusses a reduction in data throughput:

> "Still other embodiments use different methods for varying the current use by the memory. Device. For example, setting the mode control bit to a low power mode may increase the time between programming pulses that ***data throughput is reduced***." Round Rock Claim Construction Br., at 20 (citing '053 patent at 5:4-9) (emphasis added).

3. Round Rock's Construction Removes Limitations from the Claim

Round Rock's construction attempts to read out limitations of the claims.[48] For example,

[48] This is highlighted in Round Rock's citation to the specification where they emphasize "varying the current use" (i.e., adjustable current consumption") and "setting the mode control bit to a low power

claim 1 recites, in part, (i) an adjustable current; (ii) a low power mode; and (iii) a mode control bit.

> A memory device having an adjustable current consumption, the memory device comprising:
> a memory array for storing data input to the memory device during a low power mode; and
> a data register that stores a mode control bit, the adjustable current consumption being set to the low power mode in response to a state of the mode control bit.

Round Rock's construction of "adjustable current consumption being set to the low power mode" to be "setting the device to a mode for low current consumption" effectively reads either the "adjustable current consumption" or "the low power mode." As previously explained, the adjustable current consumption is related to the current consumed and the low power mode is the mode in which the lower current consumption is achieved. Round Rock is attempting to replace two elements, "adjustable current consumption" and "low power mode" with one.

Accordingly, the court should construe "adjustable current consumption being set to the low power mode in response to a state of the mode control bit" to mean "the amount of current consumed being dependent on the chosen mode as determined by the state of a mode control bit, where the mode chosen is one in which a reduced quantity of bits is programmed at once."

4. Constructions as they relate to summary judgment

In its infringement contentions, Round Rock has pointed to no mode in which a reduced quantity of bits is programmed at once. Thus, if ASUS's construction is adopted, summary judgment of non-infringement would be proper on all asserted claims containing the disputed phrase.

IX. CONCLUSION

For the foregoing reasons, ASUS respectfully requests that the Court adopts ASUS's constructions of the disputed terms.

mode" ("i.e., the "mode control bit" and "low power mode"). *See* Round Rock Claim Construction Br., at 20.

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